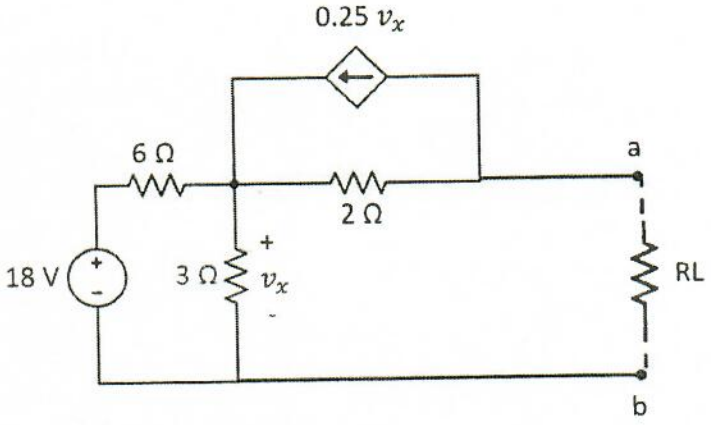
Problem : P1 Area Circuit I Student Code____

For the circuit below, find and sketch the Norton Equivalent circuit with respect to the terminals 'a' and 'b'. (25 pts.)



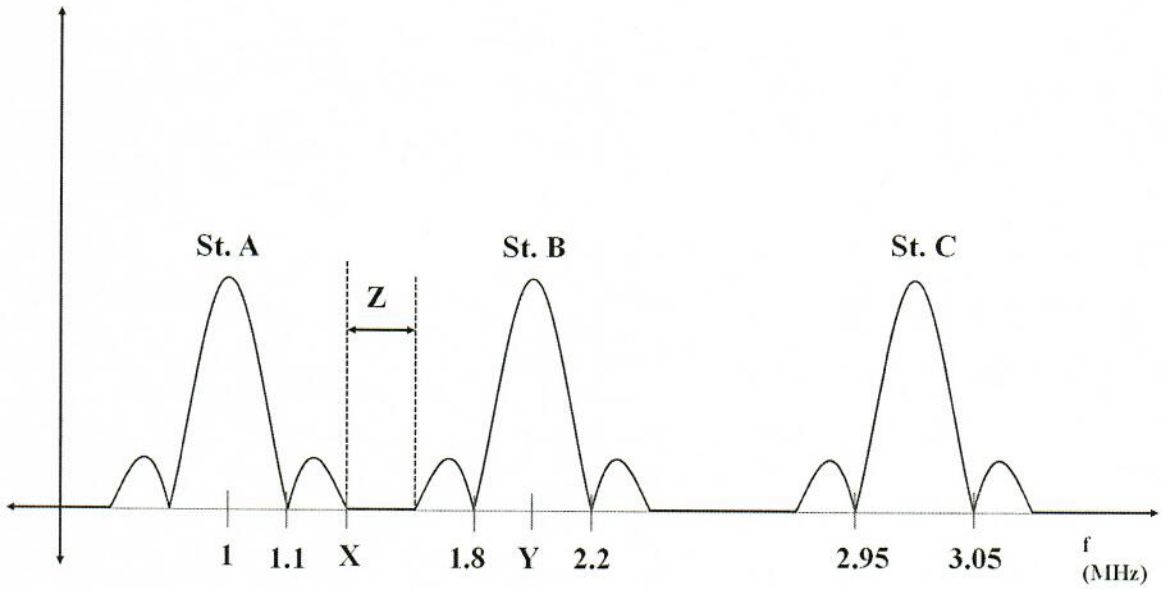
Problem: 4 Area Circuits/Electronics Student Code____

P4

Design and draw a two-input CMOS NAND schematic logic circuit showing both NMOS and PMOS explicitly. Also, construct the truth table. Assume that the two inputs are "A" and "B" and the output is "v_o".

Problem : P7 Area: Communications/Signal Processing Student Code:

Consider the below seen spectral analysis which shows multiple stations (St.) employing BPSK transmission created by modulating an NRZ-L baseband wave with the carrier wave. Note only the simplified and limited-spectrum version of the actual spectral profiles are shown below.



1) Using the spectrum shown above, answer the following questions.
   a) Calculate the value of X.
   b) Calculate the value of Y.
   c) Calculate the value of Z.
   d) Calculate the data rate for station A.
   e) Calculate the data rate for station B.
   f) Calculate the data rate for station C.
   g) Calculate the signal bandwidth for station A.

2) Consider the 16QAM passband communication system. If the symbol rate is 10 M symbols/s, calculate the data rate.

Problem : P8 **Area:** Communications/Signal Processing **Student Code:**

Consider a CT signal $x(t) = \cos(200\pi t)$. A sampling frequency, fs, is used to sample this signal to generate a DT signal x[n]. A spectral analysis is performed on x[n]. For each value of sampling frequency mentioned below, calculate the observed normalized positive discrete frequency in the spectral analysis. Note, the value of the normalized discrete frequency must be between 0 and 0.5.

a) fs = 175 Hz

b) fs = 75 Hz

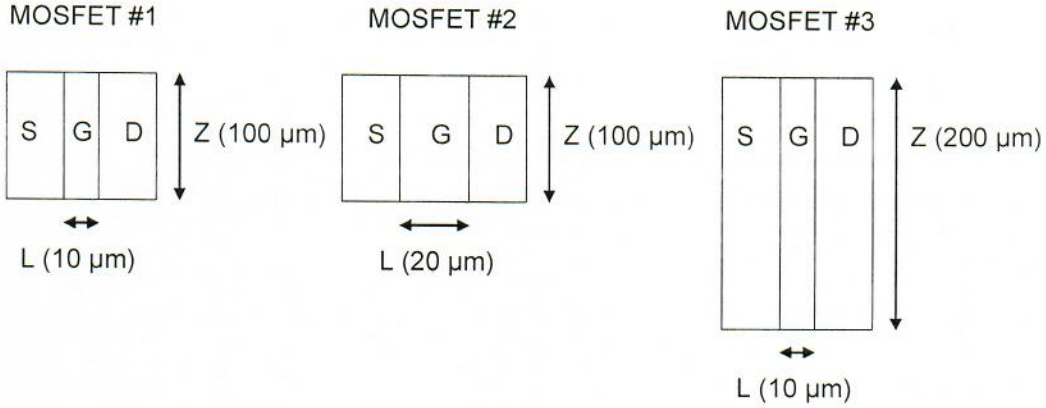
c) fs = 45 Hz

d) fs = 60 Hz

e) fs = 225 Hz

Problem : P19 **Area:** Waves/Devices **Student Code:**

Three different MOSFET layouts are shown. For all three MOSFETs, the thickness (0.9 nm) and resistivity (1.0×10^{-3} Ωcm) of their inversion layers are uniform over the entire gate region.



< Figure. 1 Top View of Different MOSFETS >

a. Calculate the conductance of the inversion layer of each MOSFETs in Figure 1. (at $V_{DS} = 0$ V, i.e. the inversion layer thickness does not change).

b. If the drain-source current I_{DS} of MOSFET #1 is 12 mA at a given operational conditions (e.g. drain-source voltage V_{DS} and a gate-source voltage V_{GS}, etc.), calculate I_{DS} of #2 and #3 MOSFETs at the same conditions.

Constants*		**Equations (p-type substrate MOSFET)***	
$kT = 0.0259$ [eV]	(at 300 K)	$\Psi_{s(inv)} = 2\Psi_B = (2kT / q)\ln(p_{po} / n_i)$	
Si Bandgap = 1.12 [eV] (at 300 K)		$W_m = \sqrt{(2\varepsilon_s\Psi_{s(inv)} / qN_A)}$	
Intrinsic carrier concentration of Silicon = 1×10^{10} [cm^{-3}] (at 300 K)		$V_T = V_o + \Psi_{s(inv)}$	
$N_c = 2.86\times10^{19}$ [cm^{-3}]	(at 300 K)	$V_T = qN_AW_m / C_o + \Psi_{s(inv)} = \sqrt{(2\varepsilon_sqN_A\Psi_{s(inv)})} / C_o + \Psi_{s(inv)}$	
$N_v = 2.66\times10^{19}$ [cm^{-3}]	(at 300 K)	$V_{FB} = \varphi_{ms} - (Q_f + Q_m + Q_{ot}) / C_o$	
Elementary charge = 1.6×10^{-19} [C]		$R = \rho L/A$	
$\varepsilon_o = 8.85E{-}14$ [F/cm]		$I_D = (Z / L)\mu_nC_o(V_G - V_T)V_D$	(when $V_D < V_G - V_T$)
$\varepsilon_s = 11.9\ \varepsilon_o$ [F/cm]	(Si)	$I_D = (Z / 2L)\mu_nC_o(V_G - V_T)^2$	(when $V_D \geq V_G - V_T$)
$\varepsilon_{ox} = 3.9\ \varepsilon_o$ [F/cm]	(SiO_2)		

* Definition of parameters are not provided. It is expected that the examinee interprets the meaning.

Problem: 20 **Area: Waves and Devices** **Student Code**____

A coaxial cable is filled with a lossy dielectric. The fields inside the coax are given (in cylindrical coordinates) by the following equations.

$$\vec{E}(\rho, z) = \hat{\rho}\frac{e^{j\beta z}e^{-\alpha z}}{\rho}$$
$$\vec{H}(\rho, z) = \hat{\phi}\frac{e^{j\beta z}e^{-\alpha z}}{\eta\rho}$$

where η is the complex intrinsic impedance of the dielectric material and is a complex number written in polar form as $\eta = |\eta|e^{j\phi}$.

a. Find the complex Poynting vector
b. Find the complex power that is flowing in the positive z direction at any point z on the coax.

Problem: P21 **Area**: Computational Intelligence **Code #**_____

(a) Describe how AI has been integrated into two products/applications that you commonly use.

(b) Define Artificial Intelligence (AI) and Computational Intelligence (CI). Describe two similarities and two differences between AI and CI.

Problem: P22 Area: Computational Intelligence **Code #**_____

Answer the questions for parts a, b, and c below.

(a) Define each of the following: supervised, unsupervised learning and reinforcement learning

(b) Define data augmentation and regularization and how they relate to the use of Computational Intelligence techniques.

Problem: P24 **Area**: Computational Intelligence **Code #**_____

Answer the follow questions.

When applying CI techniques to a given dataset, the dataset may be broken up into training, cross-validation, and test sets. Describe the process of applying a CI technique to a training data set to determine whether the CI technique has been overtrained. What are indicator(s) that a CI technique has been overtrained? What is role of a cross-validation data set in the training process of a CI technique? What are two commonly used metrics for evaluating the CI technique test set results?

Problem: 28 **Area Computer Architecture and Embedded Systems**

Student Code____

a) Within the scope of pipelining, define the term of hazard.

b) Name different types of hazards.

c) For each type of hazard named in (b) name and briefly describe two solutions to overcome its effect.

Problem: P29 **Area: Integrated Circuits and Logic Design** **Code #_____**

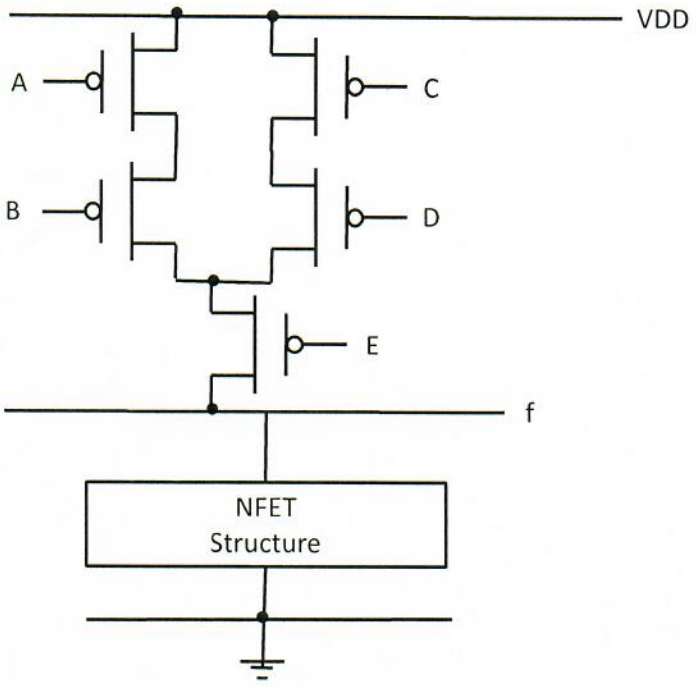
Answer the questions for parts **a** and **b** below.

a. Simplify the logic expression $F(\mathrm{a,b,c}) = (a + \overline{b})(\overline{c} + \overline{b})(\mathrm{a}+\overline{b}+\mathrm{c})$ using **algebraic manipulation** to obtain a logic expression that uses as few gates as possible (exclude inverters from the total gate count). Individual gates are not restricted on the number of inputs. *Show your work for full credit.* DO NOT USE K-MAPS.

b. Construct the truth table for $F(\mathrm{a,b,c}) = (a + \overline{b})(\overline{c} + \overline{b})(\mathrm{a}+\overline{b}+\mathrm{c})$.

Problem: P30 **Area: Integrated Circuits and Logic Design** **Code #_____**

Consider a partial CMOS structure shown below.



a) Draw the missing nFET array. Note that the pFET array does not need to be redrawn.
b) Write a Boolean expression for f

Problem: P31 **Area: Integrated Circuits and Logic Design** **Code #_____**

Design a 3-bit down counter 75316420... using D flip-flops, including drawing the counter circuit. Show your design steps for full credit.

Problem: P32 **Area: Integrated Circuits and Logic Design** **Code #_____**

Draw a circuit to implement the function $f(w,x,y,z) = \sum m\,(0,2,3,4,7,9,11,12,13)$ using a 4:1 MUX and other logic gates as needed. You may use the truth table to help if needed.

w	x	y	z	f
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Problem: P33 **Area: Networking, Security, and Dependability** **Student Code: ____**

This problem has two parts. For full credit, you must answer both parts correctly.

Part of a networking infrastructure consists of three routers, R1, R2, and R3; and six networks, N1 through N6, as shown in the figure below. The routing table for each router is as shown in the figure.

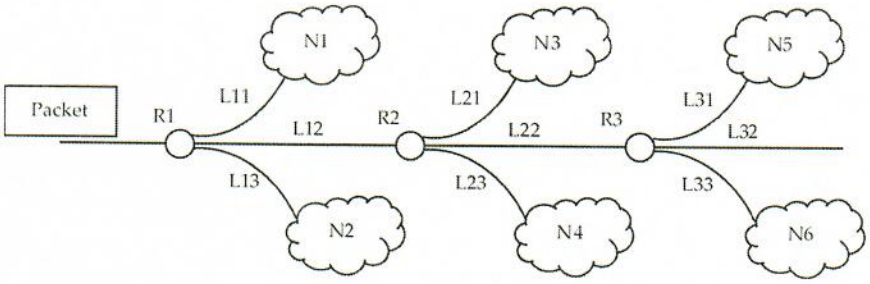
A packet with destination IP address 195.25.11.8 arrives at router R1. Answer both parts below.
Show your work. You will receive no credit for an answer unless you clearly show how you arrived at it.

You may find some of the following information useful:
17D = 11H, 25D = 19H, 32D = 20H, 48D = 30H, 57D = 39H, 67D = 43H, 96D = 60H, 100D = 64H, 104D = 68H, 112D = 70H, 120D = 78H, 135D = 87H, 168D = A8H, 192D = C0H, 199D = C7H, 204D = CCH, 226D = E2, 255D = FFH

R1 Table Entry	Link
195.25.0.0/21	L11
195.25.10.0/23	L12
195.25.8.0/22	L13
195.25.16.0/20	L13

R2 Table Entry	Link
195.25.16.0/20	L21
195.25.24.0/19	L22
111.25.8.0/22	L23

R1 Table Entry	Link
default	L31
195.25.3.0/24	L32
195.25.16.0/20	L33



a. How is the packet routed by router R1, R2, and R3, respectively? Show your work.

b. Assume that we want to partition the 195.25.3.0/24 space into three departments, A, B, and C, which have 90, 30, and 110 hosts, respectively. The addresses for each department should be consecutive. We want to divide the space into no more than four non-overlapping parts, each of which can be of a different size. Ignore all reserved addresses. Show the prefix/length CIDR mask for the address space(s) allocated to each department. You should have no more than four masks. No additional IP addresses can be acquired. Show every step of your work.

Problem: P36 Area: Networking, Security, and Dependability **Student Code: ____**

This problem has six parts. For full credit, you must answer all six parts correctly.

Answer all of the following questions. Brief answers suffice.

a. Explain the difference between statistical anomaly detection and rule-based intrusion detection.

b. Explain how the public and private key, respectively, are used in asymmetric encryption.

c. Explain how the public and private key, respectively, are used in digital signatures.

d. Describe a replay attack. Is it a passive or active attack? Explain your answer.

e. Assume that we suddenly gain a thousand-fold increase in computing power, i.e., can perform arithmetic operations a thousand times more quickly. How does this threaten the security of symmetric encryption schemes? How about asymmetric encryption schemes?

f. Assume that we suddenly discover a much quicker method to factor large numbers. This is an increase in mathematical knowledge, not sheer computing power. Which aspects of cybersecurity will be affected?